least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor.

56. (New) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

57. (New) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

58. (New) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

59. (New) The method of claim 56 wherein said step of providing doped silicon regions further comprises forming two memory cells.

60. (New) The method of claim 59 further comprising connecting a central region of said seven-region planar thyristor to a shared row address line.

61. (New) The method of claim 55 wherein said step of providing doped silicon regions further comprises forming one memory cell.

Please rewrite claim 48 as follows:

Replacement Claims

48. (Twice Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor.